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DARBY & DARBY P.C.
P.O. BOX 5257
NEW YORK, NY 10150-5257

EXAMINER	
KUMAR, PANKAJ	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,095	MEDLOCK ET AL.	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33-37* is/are allowed.

6)☒ Claim(s) *1-9,15-19,21-25 and 27* is/are rejected.

7)☒ Claim(s) *10-14,20,26 and 28-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/28/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: Applicant should fill in the blanks in the specification in the area where it is cross-referencing related applications. Appropriate correction is required.

Drawings

2. It is noted the applicant filed substitute drawings on 9/26/2001.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 6, 8, 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozcelik USPN 6,233,277. Here is how the reference teaches the claims:

5. As per claim 1: An apparatus for processing data in a spread spectrum system (preamble is not afforded patentable weight), comprising: a decimation circuit (Ozcelik fig. 4: 56) having an associated decimation factor (not in Ozcelik but would be obvious as explained below); a memory coupled to said decimation circuit (Ozcelik fig. 4: 40); and an interpolation circuit coupled to said memory (Ozcelik fig. 4: 82), said interpolation circuit having an associated interpolation factor (not in Ozcelik but would be obvious as explained below); wherein said decimation circuit (Ozcelik fig. 4: 56) decimates a data rate of received data by said decimation

factor to a decimated rate and stores said received data into said memory (Ozcelik fig. 4: 82) at said decimated rate; and wherein said interpolation circuit interpolates (Ozcelik fig. 4: 82) said decimated rate by said interpolation factor to an interpolated rate and retrieves said received data from said memory (Ozcelik fig. 4: 82) at said interpolated rate.

6. What Ozcelik does not teach is that the decimator (Ozcelik fig. 4: 56) has a decimation factor and decimation rate and that the interpolator (Ozcelik fig. 4: 82) has an interpolation factor and an interpolated rate. The office takes official notice that a decimator has a decimation factor with which it decimates to a decimation rate to decimate or reduce the amount of the data and that an interpolator has an interpolation factor to which it interpolates to an interpolated rate to interpolate or increase or boost amount of data. Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to modify the prior art teaching of Ozcelik with the decimator (Ozcelik fig. 4: 56) having a decimation factor and decimation rate and the interpolator (Ozcelik fig. 4: 82) having an interpolation factor and an interpolated rate as indicated by the instant claims, because Ozcelik suggests decimation and interpolation in the analogous art of processing data by decimation and interpolation.

7. The spread spectrum recitation is not given patentable weight since the recitation occurs in the preamble and recites the intended use of a structure and the body of claim does not depend on the preamble for completeness and the bodily limitations are able to stand alone. Thus, the bodily limitations do not require a spread spectrum system as the bodily limitations can be comprised in a video system such as the one in Ozcelik.

8. As per claim 2: The apparatus of claim 1, further comprising: a communication processor (Ozcelik fig. 1: transmission system and receiver comprise communication; HDTV systems have

processors in order to encode the source by compression and decode the received for display; col. 1 line 61: decoding process, col. 2 lines 6-10: processing compression) coupled to said interpolation circuit (Ozcelik fig. 1: 30 coupled to receiver which is coupled to transmitter; fig. 2: 46 and 48 are part of 30; fig. 4: decimator and interpolator are part of 46 and 48 respectively) for receiving data from said memory at said interpolated rate.

9. As per claim 3: The apparatus of claim 1, further comprising: a dedicated controller for controlling data retrieval from said memory (Ozcelik fig. 4: 86 is dedicated to control the retrieval of the value C from memory 40).

10. As per claim 4: The apparatus of claim 1, further comprising: a micro-processor for controlling data retrieval from said memory (Ozcelik fig. 4:86 is part of the decoder fig. 1: 30 and 86 retrieves data from memory and col. 2 lines 30-33 or paragraph 12 teaches that the decoder is part of the processor: col. 2 lines 30-33 or paragraph 12: "Thus, the video decoder of the present invention provides better picture quality than other known decoding processes where the processor is limited." Ozcelik does not teach that the processor is a micro-processor. The office takes official notice that processors are small and hence microprocessors as they are widely prevalent in microcomputers and various electronics in general. Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to modify the prior art teaching of Ozcelik with the processor being a microprocessor as recited by the instant claims, because Ozcelik suggests reducing size, such as reducing size of memory in the analogous art of data processing.

11. As per claim 6. The apparatus of claim 1, wherein said decimation factor is hard-coded into said decimation circuit (Ozcelik col. 1 lines 43-45: "predetermined decimation scheme";

since it is predetermined, it is hard-coded as opposed to adaptively changed in the processors or Ozcelik).

12. As per claim 8. The apparatus of claim 1, wherein said interpolation factor is hard-coded into said interpolation circuit (not in Ozcelik but would be obvious). Ozcelik teaches the interpolation circuit but does not teach that its interpolation factor is hard coded. The office takes official notice that memory space is limited. Accordingly, enough interpolation needs to be done in order to obtain good quality for the data to be understandable and hence the size of the memory in Ozcelik will be partially dependent on an interpolation factor that would result in good quality as there would be a boost or increase of data which the memory would be expected to hold. Also, hard coded variable costs less when developing a system than a programmable variable and interpolation has an interpolation factor (as discussed above with respect to claim 1). Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to modify the prior art teaching of Ozcelik with the hard-coded interpolation factor as recited by the instant claims, because Ozcelik suggests a maximum memory size which would be partially dependent on an interpolation factor and an inexpensive system in the analogous art of processing by interpolation.

13. As per claim 21. A method for processing data in a spread spectrum system, comprising the steps of: receiving data at a sampling rate (Ozcelik fig. 2: inherent for digital data 22 to be sampled and thus have a sampling rate); decimating (Ozcelik fig. 4: 56) said sampling rate by a decimation factor (not in Ozcelik but would be obvious as explained below) to obtain a decimated rate (Ozcelik fig. 4: output of 56); storing said data into a memory at said decimated rate (Ozcelik fig. 4: 82); interpolating said decimated rate to obtain an interpolated rate (Ozcelik

fig. 4: 82); and outputting said data from said memory at said interpolated rate to a communication processor (Ozcelik fig. 1: output of 30 going to display 26; since it is displaying, it is communicating).

14. What Ozcelik does not teach is that the decimator (Ozcelik fig. 4: 56) has a decimation factor and decimation rate and that the interpolator (Ozcelik fig. 4: 82) has an interpolation factor and an interpolated rate. The office takes official notice that a decimator has a decimation factor with which it decimates to a decimation rate to decimate or reduce the amount of the data and that an interpolator has an interpolation factor to which it interpolates to an interpolated rate to interpolate or increase or boost amount of data. Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to modify the prior art teaching of Ozcelik with the decimator (Ozcelik fig. 4: 56) having a decimation factor and decimation rate and the interpolator (Ozcelik fig. 4: 82) having an interpolation factor and an interpolated rate as indicated by the instant claims, because Ozcelik suggests decimation and interpolation in the analogous art of processing data by decimation and interpolation.

15. Ozcelik teaches decimating but does not teach decimating said sampling rate. The office takes official notice that when a decimator is receiving samples at a sampling rate, that the decimator is reducing the number of samples by picking every x sample which reduces or decimates the sampling rate. Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to modify the prior art teaching of Ozcelik with the decimator decimating said sampling rate as recited by the instant claims, because Ozcelik suggests the decimator in fig. 4: 56, 46 is receiving digital samples via other components in fig. 2 22 to 46 in the analogous art of processing data by decimation.

16. The spread spectrum recitation is not given patentable weight since the recitation occurs in the preamble and recites the intended use of a structure and the body of claim does not depend on the preamble for completeness and the bodily limitations are able to stand alone. Thus, the bodily limitations do not require a spread spectrum system as the bodily limitations can be comprised in a video system such as the one in Ozcelik.

17. As per claim 22. The method of claim 21, further comprising the step of: retrieving data from said memory in accordance with instructions from a micro-processor. (Ozcelik fig. 4: 86 is part of the decoder fig. 1: 30 and 86 retrieves data from memory and col. 2 lines 30-33 or paragraph 12 teaches that the decoder is part of the processor: col. 2 lines 30-33 or paragraph 12: "Thus, the video decoder of the present invention provides better picture quality than other known decoding processes where the processor is limited." Ozcelik does not teach that the processor is a micro-processor. The office takes official notice that processors are small and hence microprocessors as they are widely prevalent in microcomputers and various electronics in general. Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to modify the prior art teaching of Ozcelik with the processor being a microprocessor as recited by the instant claims, because Ozcelik suggests reducing size, such as reducing size of memory in the analogous art of data processing.

18. As per claim 23. The method of claim 21, further comprising the step of: retrieving data from said memory in accordance with instructions from a dedicated controller (Ozcelik fig. 4: 86 is dedicated to control the retrieval of the value C from memory 40).

19. Claims 5, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozcelik USPN 6,233,277 as applied to claim 1 above, and further in view of Lovinggood USPN 6,697,603. Here is how the references teach the claims:

20. As per claim 5: The apparatus of claim 1, wherein said decimation factor is programmable by configuring said decimation circuit (Ozcelik does not teach this). Lovinggood 6697603 teaches programmable decimation (Lovinggood col. 12 lines 38-39). Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to arrive at the programmable decimation as indicated by the instant claims, because the combined teaching of Ozcelik with Lovinggood suggest communications (Lovinggood col. 1 lines 43-44) with programmable decimation as indicated by the instant claims with good quality (Ozcelik col. 2 line 16). Furthermore, one of ordinary skill in the art, would have been motivated to combine the teachings of Ozcelik with Lovinggood because Ozcelik suggests decimation (something broad) in general and Lovinggood suggests the beneficial use of programmable decimation such as if too much data is removed by decimation such that the data is incomprehensible and hence not of good quality, then one would want to change the decimation factor to make the data comprehensible, and hence of good quality, in the analogous art of communication by decimation.

21. As per claim 7. The apparatus of claim 1, wherein said interpolation factor is programmable by configuring said interpolation circuit. (Ozcelik does not teach this). Lovinggood 6697603 teaches programmable interpolation (Lovinggood col. 9 lines 23-34 or paragraph 41: "The interpolation rate is also programmable via the user interface 310."). Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to

arrive at the programmable decimation as indicated by the instant claims, because the combined teaching of Ozcelik with Lovinggood suggest communications (Lovinggood col. 1 lines 43-44) with programmable interpolation as indicated by the instant claims. Furthermore, one of ordinary skill in the art, would have been motivated to combine the teachings of Ozcelik with Lovinggood because Ozcelik suggests interpolation (something broad) in general and Lovinggood suggests the beneficial use of programmable interpolation such as the interpolation rate being equal to the decimation rate (Lovinggood col. 9 lines 21-23 or paragraph 41: "Generally, the interpolation rate is equal to the decimation rate used for the digital decimator 530.") and thus when the decimation rate changes, the interpolation rate changes in the analogous art of communication by decimation.

22. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozcelik USPN 6,233,277 as applied to claim 1 above, and further in view of McDonough USPN 5,778,024. Here is how the references teach the claim:

23. As per claim 9: The apparatus of claim 1, wherein said memory is a single port RAM (not in Ozcelik). Ozcelik does not teach that the memory is a single port RAM. McDonough 5778024 teaches memory being single port RAM (McDonough col. 18 lines 54-55). Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to arrive at the memory being single port RAM as recited by the instant claims, because the combined teaching of Ozcelik with McDonough suggest memory being single port RAM as recited by the instant claims. Furthermore, one of ordinary skill in the art, would have been motivated to combine the teachings of Ozcelik with McDonough because Ozcelik suggests

memory (something broad) in general and McDonough suggests the beneficial use of single port RAM such as using conventional techniques to transfer data (McDonough col. 18 lines 56-59) as opposed to some other type of memory such as one with multiple ports which would make data transfer complicated in the analogous art of processing data via a memory.

24. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozcelik USPN 6,233,277 as applied to claim 1 above, and further in view of Levin USPN 6,639,906. Here is how the references teach the claims:

25. As per claim 15: Ozcelik teaches the apparatus of claim 1. Ozcelik does not teach wherein said memory is a circular buffer. Levin 6639906 teaches circular buffer in fig. 12. Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to arrive at the circular buffer being the memory as indicated by the instant claims, because the combined teaching of Ozcelik with Levin suggest the memory being a circular buffer as indicated by the instant claims. Furthermore, one of ordinary skill in the art, would have been motivated to combine the teachings of Ozcelik with Levin because Ozcelik suggests memory (something broad) in general and Levin suggests the beneficial use of the memory being a circular buffer, such as replacing old samples with new samples (col. 12 lines 2-3) which saves space or memory in the analogous art of memory.

26. As per claim 16: The apparatus of claim 15, wherein said circular buffer includes multiple registers (Levin fig. 12: 1WS, 2WS, 3WS, 4WS, col. 12 lines 3-4: the capacity of the queue is sufficient to store 4 Walsh symbols.).

27. As per claim 17: The apparatus of claim 16, further comprising a plurality of despreaders (not in Ozcelik). Ozcelik does not teach a plurality of despreaders. Levin teaches a plurality of despreaders (Levin fig. 4: 130, 112). Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to arrive at the plurality of despreaders as recited by the instant claims, because the combined teaching of Ozcelik with Levin suggest a plurality of despreaders as recited by the instant claims. Furthermore, one of ordinary skill in the art, would have been motivated to combine the teachings of Ozcelik with Levin because Ozcelik suggests reception (Ozcelik fig. 1: 14) (something broad) in general and Levin suggests the beneficial use of reception by using a plurality of despreaders (such as despreading to receive a signal (Levin col. 7 lines 43-65) if the transmitted signal is spread (Levin col. 3 lines 7-23)) in the analogous art of receiver.

28. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozcelik USPN 6,233,277 in view of Levin USPN 6,639,906 as applied to claim 17 above, and further in view of Brown USPN 6,650,694. Here is how the references teach the claim:

29. As per claim 18: The apparatus of claim 17, wherein each of said plurality of despreaders includes: a selector circuit (Levin figs.5, 7: data select); and a rake finger (not in Ozcelik or Levin). Brown 6650694 teaches rake finger (Brown col. 2 line 10). Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to arrive at the despreader including a rake finger as recited by the instant claims, because the combined teaching of Ozcelik in view of Levin with Brown suggests each despreader includes a rake finger as indicated by the instant claims. Furthermore, one of ordinary skill in the art, would have been

motivated to combine the teachings of Ozcelik in view of Levin with Brown because Ozcelik in view of Levin suggests despreaders (something broad) in general and Brown suggests the beneficial use of despreader including a rake finger such as paragraph 120 in col. 35 lines 10-14: "Because most RAKE receiver functions involve correlations and accumulations, regardless of the particular wireless protocol, a centralized correlation machine can be used for various RAKE receiver tasks like finger de-spreading and search." in the analogous art of dispreading and processing data.

30. As per claim 19: The apparatus of claim 18, wherein data stored in said multiple registers (Levin fig. 12: 1WS, 2WS, 3WS, 4WS, col. 12 lines 3-4: the capacity of the queue is sufficient to store 4 Walsh symbols.) are accessible by multiple rake fingers (Brown col. 8 line 19) via selector circuits (Levin figs.5, 7: data select) in said plurality of despreaders (Levin fig. 4: 130, 112).

31. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwakiri USPN 5,889,815. Here is how the reference teaches the claim:

32. As per claim 24: An apparatus for processing data, comprising: a plurality of rake fingers (Iwakiri 5889815 fig. 8: 100.sub.21 to 100.sub.23); a memory for storing data at the input to said plurality of rake fingers (Iwakiri fig. 8: 702); and a selector circuit (Iwakiri fig. 8: 703, 709, 715) positioned between said memory (Iwakiri fig. 8: 702) and each of said plurality of rake fingers (Iwakiri 5889815 fig. 8: 100.sub.21 to 100.sub.23; one selector for each rake finger); wherein said plurality of rake fingers (Iwakiri 5889815 fig. 8: 100.sub.21 to 100.sub.23) can access said

memory (Iwakiri fig. 8: 702) substantially simultaneously via a respective selector circuit (Iwakiri fig. 8: 703, 709, 715).

33. Iwakiri does not teach that the rake fingers can access memory substantially simultaneously. The office takes official notice that when devices in parallel are accessing the same element, they can access the element simultaneously in order to take advantage of parallelism such as increased processor speed. Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to modify the prior art teaching of Iwakiri with the rake fingers accessing memory substantially simultaneously as recited by the instant claims, because Iwakiri suggests parallel connection between the rake fingers and the memory in the analogous art of processing data.

34. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwakiri USPN 5,889,815 as applied to claim 24 above, and further in view of Laurenti USPN 6,363,470. Here is how the references teach the claim:

35. As per claim 25: Iwakiri teaches the apparatus of claim 24. Iwakiri does not teach wherein said memory is a circular buffer including a plurality of registers. Laurenti teaches wherein said memory is a circular buffer (Laurenti 6363470 fig. 9: 802) including a plurality of registers (Laurenti col. 9 line 56). Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to arrive at the circular buffer being the memory as indicated by the instant claims, because the combined teaching of Iwakiri with Laurenti suggest the memory being a circular buffer with a plurality of registers as indicated by the instant claims. Furthermore, one of ordinary skill in the art, would have been motivated to combine the

teachings of Iwakiri with Laurenti because Iwakiri suggests memory (something broad) in general and Laurenti suggests the beneficial use of the memory being a circular buffer with a plurality of registers, such as implementing different types of computational processes (col. 1 lines 14-16) where old data is not needed and thus its space should be reused to save space or memory in the analogous art of memory.

36. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwakiri USPN 5,889,815 as applied to claim 24 above, and further in view of McDonough USPN 5,778,024. Here is how the references teach the claim:

37. As per claim 27: Iwakiri teaches the apparatus of claim 24. Iwakiri does not teach wherein said memory is a single-port RAM. McDonough 5778024 teaches memory being single port RAM (McDonough col. 18 lines 54-55). Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to arrive at the memory being single port RAM as recited by the instant claims, because the combined teaching of Iwakiri with McDonough suggest memory being single port RAM as recited by the instant claims. Furthermore, one of ordinary skill in the art, would have been motivated to combine the teachings of Iwakiri with McDonough because Iwakiri suggests memory (something broad) in general and McDonough suggests the beneficial use of single port RAM such as using conventional techniques to transfer data (McDonough col. 18 lines 56-59) as opposed to some other type of memory such as one with multiple ports which would make data transfer complicated in the analogous art of processing data via a memory.

Allowable Subject Matter

38. Claims 10-14, 20, 26, 28-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

39. Claims 33-37 are allowed. The following is a statement of reasons for the indication of allowable subject matter: The art of record does not suggest the respective claim combinations together and nor would the respective claim combinations be obvious with:

40. As per claims 33-37: each of said set of despreaders including: a block multiplexer coupled to said bus; a rake finger coupled to said cache; and wherein said set of despreaders can access samples stored in said memory substantially simultaneously via said bus.

Conclusion

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (571) 272-3011. The examiner can normally be reached on Mon, Tues, Thurs and Fri after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pankaj Kumar
Patent Examiner
Art Unit 2631

PK